IN THE CLAIMS

Please add claim 34.

Please amend claims 1, 6, 17-18, 21-22, and 31 as follows:

1. (Currently Amended) A semiconductor memory comprising:

a bank of N arrays each having a corresponding array address;

a bus providing an array address signal, a row address signal (RAS), and global timing signals; and

N tracking circuits, each coupled between an associated different one of the N arrays and the bus, wherein a first tracking circuit, in response to receiving a first array address for a first array via the array address signal and a first active state of the RAS, couples the first array to the bus such that only the first array receives and responds to a first sequence of global timing signals associated with the first array address and first active state of the RAS and constituting a first bank transaction, and a second tracking circuit, in response to receiving a second array address for a second array via the array address signal and a second active state of the RAS, couples the second array to the bus such that only the second array responds to a second sequence of global timing signals associated with the second array address and second active state of the RAS and constituting a second bank transaction before the first bank transaction is complete.

2. (Original) The memory of claim 1, wherein the second array is different from and non-adjacent to the first array.

3. (Original) The memory of claim 1, wherein the semiconductor memory comprises a random access memory (RAM) device.

4. (Original) The memory of claim 1, wherein the semiconductor memory comprises a dynamic random access memory (DRAM) device.

5. (Original) The memory of claim 1, wherein each tracking circuit is further configured to provide a wait signal in response to receving an array address of its associated array and an active state of the RAS prior to completion of an ongoing transaction to its associated array or an adjacent array.

6. (Currently Amended) ~~The memory of claim 1, wherein each tracking circuit further comprises~~A semiconductor memory comprising:

a bank of N arrays each having a corresponding array address;

a bus providing an array address signal, a row address signal (RAS), and timing signals; and

N tracking circuits, each coupled between an associated different one of the N arrays and the bus, wherein a first tracking circuit, in response to receiving a first array address for a first array via the array address signal and a first active state of the RAS, couples the first array to the bus such that only the first array responds to a first sequence of timing signals constituting a first bank transaction, and a second tracking circuit, in response to receiving a second array address for a second array via the array address signal and a second active state of the RAS, couples the second array to the bus such that only the second array responds to a second sequence of timing signals constituting a second bank transaction before the first bank transaction is complete, wherein each tracking circuit comprises:

a wordline block providing a first tracking signal having an active state in response to a local RAS having an active state representative of the array address signal having the array address of its associated array and to an active state of the RAS, and providing to its associated array a local wordline pulse in response to the first tracking signal having the active state and receiving a global wordline timing signal pulse via the bus;

a sense amp block providing a second tracking signal having an active state in response to the local wordline pulse, and providing to its associated array a local sense amp pulse in response to the second tracking signal having the active state and receiving a global sense amp timing signal pulse via the bus; and

a column block providing to its associated array a local column select signal having an active state in response to the local sense amp pulse.

7. (Original) The memory of claim 6, wherein the wordline block comprises:

a flip-flop providing the first tracking signal having the active state in response to local RAS having the active state; and

an AND-gate providing the local wordline pulse in response to the global wordline timing pulse and the first tracking signal having the active state.

8. (Original) The memory array of claim 7, wherein the flip-flop sets the first tracking signal to an inactive state in response to the local wordline pulse.

9. (Original) The memory of claim 6, wherein the sense amp block comprises:

a flip-flop providing the second tracking signal having the active state in response to local wordline on pulse; and

an AND-gate providing the local sense amp pulse in response to the global sense amp timing signal pulse and the second tracking signal having the active state.

10. (Original) The memory of claim 9, wherein the flip-flop sets the second tracking signal to an inactive state in response to the local sense amp pulse.

11. (Original) The memory of claim 6, wherein the column block comprises:

a flip-flop providing the local column select signal having the active state in response to the local sense amp pulse.

12. (Original) The memory of claim 11, wherein the flip-flop sets the local column select signal to an inactive state in response to a global precharge timing signal pulse or a global sense amp timing signal pulse when the local column select signal has the active.

13. (Original) The memory of claim 12, wherein the column block further comprises:

a NOR-gate receiving the local column select signal and a sense amp operation signal indicating completion of sense amp operations to the associated array and providing a sense amp stop signal having an active state to the associated array in response to the local column select signal having the inactive state and the sense amp operation signal indicating completion of sense amp operation to the associated array.

14. (Original) The memory of claim 13, wherein the tracking circuit further comprises:

a conflict block providing a wait signal having an active state in response to the array address signal having the array address of its associated array and to an active state of the RAS prior to completion of an on-going transaction to its associated memory array.

15. (Original) The memory of claim 14, wherein the conflict block comprises:

a flip-flop providing an array operation signal having an active state representative of an ongoing transaction to its associated array; and

an AND-gate providing the wait signal in response to the operation signal having the active state and to an active state of the RAS and the array address signal having the array address of its associated array.

16. (Original) The memory of claim 15, wherein the flip-flop sets the operation signal to an inactive state in response to the sense amp stop signal having the active state and causing the wait signal to have an inactive state.

17. (Currently Amended) A tracking circuit for a semiconductor memory including a bank of N memory arrays and a bus providing an array address signal, a row address signal (RAS), and global timing signals, the tracking circuit coupled between the bus and ~~an associated~~a first memory array and configured to couple the ~~associated~~first memory array to the bus in response to receiving ~~an~~first array address for the ~~associated~~first memory array via the array address signal and an active state of the RAS such that the ~~associated~~first memory array receives and responds

to only a first sequence of global timing signals associated with the first array address and active state of the RAS and constituting a transaction ~~to~~with the ~~associated~~first memory array, ~~so that~~to enable ~~a transaction constituting~~ a second sequence of global timing signals constituting a transaction with a ~~to~~ second memory array in the bank ~~can~~to begin prior to completion of the transaction ~~to~~with the ~~associated~~first memory array.

18. (Currently Amended) The circuit of claim 17, wherein the second memory array is different from and non-adjacent to the first memory array.

19. (Original) The circuit claim 17, wherein the semiconductor memory comprises a random access memory (RAM) device.

20. (Original) The circuit 17, wherein the semiconductor memory comprises a dynamic random access memory (DRAM) device.

21. (Currently Amended) The circuit of claim 17, wherein ~~each~~the tracking circuit is further configured to provide a wait signal in response to receving an array address of ~~its associated~~the first memory array and an active state of the RAS prior to completion of an ongoing transaction ~~to its associated~~with the first memory array or an adjacent memory array.

22. (Currently Amended) ~~The circuit of claim 17, wherein the each tracking circuit further comprises:~~A tracking circuit for a semiconductor memory including a bank of N memory arrays and a bus providing an array address signal, a row address signal (RAS), and timing signals, the tracking circuit coupled between the bus and an associated memory array and configured to couple the associated memory array to the bus in response to receiving an array address for the associated memory array via the array address signal and an active state of the RAS such that the associated memory array responds to only a first sequence of timing signals constituting a transaction to the associated memory array, to enable a transaction constituting a second

sequence of timing signals to second memory array in the bank to begin prior to completion of the transaction to the associated memory array, the tracking circuit comprising:

a wordline block providing a first tracking signal having an active state in response to a local RAS having an active state representative of the array address signal having the array address of its associated array and to an active state of the RAS, and providing to its associated array a local wordline pulse in response to the first tracking signal having the active state and receiving a global wordline timing signal pulse via the bus;

a sense amp block providing a second tracking signal having an active state in response to the local wordline pulse, and providing to its associated array a local sense amp pulse in response to the second tracking signal having the active state and receiving a global sense amp timing signal pulse via the bus; and

a column block providing to its associated array a local column select signal having an active state in response to the local sense amp pulse.

23. (Original) The circuit of claim 22, wherein the wordline block comprises:

a flip-flop providing the first tracking signal having the active state in response to local RAS having the active state; and

an AND-gate providing the local wordline pulse in response to the global wordline timing pulse and the first tracking signal having the active state.

24. (Original) The circuit array of claim 23, wherein the flip-flop sets the first tracking signal to an inactive state in response to the local wordline pulse.

25. (Original) The circuit of claim 22, wherein the sense amp block comprises:

a flip-flop providing the second tracking signal having the active state in response to local wordline on pulse; and

an AND-gate providing the local sense amp pulse in response to the global sense amp timing signal pulse and the second tracking signal having the active state.

26. (Original) The circuit of claim 25, wherein the flip-flop sets the second tracking signal to an inactive state in response to the local sense amp pulse.

27. (Original) The circuit of claim 22, wherein the column block comprises:

a flip-flop providing the local column select signal having the active state in response to the local sense amp pulse.

28. (Original) The circuit of claim 27, wherein the flip-flop sets the local column select signal to an inactive state in response to a global precharge timing signal pulse or a global sense amp timing signal pulse when the local column select signal has the active.

29. (Original) The circuit of claim 28, wherein the column block further comprises:

a NOR-gate receiving the local column select signal and a sense amp operation signal indicating completion of sense amp operations to the associated array and providing a sense amp stop signal having an active state to the associated array in response to the local column select signal having the inactive state and the sense amp operation signal indicating completion of sense amp operation to the associated array.

30. (Original) The circuit of claim 29, wherein the tracking circuit further comprises:

a conflict block providing a wait signal having an active state in response to the array address signal having the array address of its associated array and to an active state of the RAS prior to completion of an on-going transaction to its associated memory array.

31. (Currently Amended) A method of increasing bandwidth of a semiconductor memory having a plurality of arrays each having an array address and a bus providing an array address signal, a row address signal (RAS), and global timing signals, the method comprising:

coupling a first array of the plurality to the bus in response to the bus providing an array address of the first array via the array address signal and a first active state of the RAS such that only the first array ~~to the bus such that only the first array~~ receives and responds to a first

sequence of global timing signals associated with the first array address and first active state of the RAS and constituting a first bank transaction; and

coupling a second array of the plurality to the bus in response to the bus providing an array address of the second array via the array address signal and a second active state of the RAS such that only the second array receives and responds to a second sequence of global timing signals associated with the second array address and second sctive state of the RAS and constituting a second bank transaction before the first bank transaction is complete.

32. (Original) The method of claim 31, wherein the first and second arrays are different and non-adjacent arrays in a same memory array bank.

33. (Original) The method of claim 31, wherein the semiconductor memory comprises a dynamic random access memory (DRAM) device.

34. (New) A method of increasing bandwidth of a semiconductor memory having a plurality of arrays each having an array address and a bus providing an array address signal, a row address signal (RAS), and timing signals, the method comprising:

coupling a first array of the plurality to the bus in response to the bus providing an array address of the first array via the array address signal and a first active state of the RAS such that only the first array to the bus such that only the first array responds to a first sequence of timing signals constituting a first bank transaction;

coupling a second array of the plurality to the bus in response to the bus providing an array address of the second array via the array address signal and a second active state of the RAS such that only the second array responds to a second sequence of timing signals constituting a second bank transaction before the first bank transaction is complete; and

wherein coupling an array to the bus includes:

providing a first tracking signal having an active state in response to a local RAS having an active state representative of the array address signal having the array address of its associated array and to an active state of the RAS, and providing to its

associated array a local wordline pulse in response to the first tracking signal having the active state and receiving a global wordline timing signal pulse via the bus;

providing a second tracking signal having an active state in response to the local wordline pulse, and providing to its associated array a local sense amp pulse in response to the second tracking signal having the active state and receiving a global sense amp timing signal pulse via the bus; and

providing to its associated array a local column select signal having an active state in response to the local sense amp pulse.